

Application No. 09/943,094
Reply to Office Action of June 10, 2003
Amendment Dated September 9, 2003

Attorney Docket No. 81751.0017

REMARKS

Applicant appreciates the thorough examination of the application that is reflected in the Office Action dated June 10, 2003. Claim 12 is cancelled without prejudice or disclaimer. Claims 1, 7 and 14 are amended; marked up versions of the amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). Independent claims 1, 7 and 14 have been amended to further distinguish over the cited references. New dependent claims 32-44 are added by this amendment. Claims 1-11, 13-19 and 32-44 are pending in the application. Reexamination and reconsideration of the application, as amended, are respectfully requested.

Art-based Rejections

Claims 1-3, 7, 8, 12, and 14-18 were rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Patent Number JP-11-54758 to Wakahara et al. (hereinafter "Wakahara"). Claims 1, 2, 4, 7, 8, and 12 were rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Number 6,372,652 to Matsumoto (hereinafter "Matsumoto"). Claims 1, 2, 4, and 7-11 were rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Number 6,407,429 to Ko et al (hereinafter "Ko"). Claims 14-16 were rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,888,854 to Morihara (hereinafter "Morihara"). Claim 5 was rejected under 35 U.S.C. 102(e) as being unpatentable over Matsumoto in view of Japanese Patent Number JP-2000-216400 to Yoshida (hereinafter "Yoshida"). Claims 6, 13, and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wakahara in view of US Patent Number 6,511,879 to Drynan et al (hereinafter "Drynan").

Applicant respectfully traverses these rejections for at least the following reasons.

Application No. 09/943,094
Reply to Office Action of June 10, 2003
Amendment Dated September 9, 2003

Attorney Docket No. 81751.0017

Claims 1-6

To assist the Examiner in understanding how claim 1 reads on an embodiment of the invention shown, for example, in FIG. 1, Applicant has annotated claim 1 below. This embodiment is discussed, for example, at page 9, lines 20-26 of the specification. Applicant notes that the claims should not be construed as being limited to this embodiment, and that the annotation is provided only for the purpose of showing the Examiner how claim 1 reads on this embodiment. Amended claim 1 relates to a semiconductor device (FIG. 1), comprising:

a semiconductor substrate (120) having a first conductive layer (122) provided therein;

an insulation layer (130) provided above the semiconductor substrate(120);

a semiconductor layer (140) provided above the insulation layer (130);

a second conductive layer (162) disposed in contact with the semiconductor layer (160), and electrically connected to the first conductive layer (122); and

a contact layer (160) provided in a first connection hole (150), the contact layer (160) electrically connecting the first conductive layer (122) and the second conductive layer (162). (Emphasis added.)

Applicant submits that the cited references fail to teach or suggest, for example, "a second conductive layer disposed in contact with the semiconductor layer," as required by claim 1.

For example, as shown in FIG. 2 of the Wakahara reference, the silicon layer 1c is not in contact with the wiring 12d. Rather, structures such as the field insulating film 2 and the interlayer insulating film 10 are disposed between the silicon layer 1c and the wiring 12d.

There is nothing shown in FIGS. 4A and 4B of the Matsumoto reference that corresponds to the claimed "second conductive layer." Moreover, neither the metal interconnections nor the conductive plugs that would eventually fill the contact

Application No. 09/943,094
Reply to Office Action of June 10, 2003
Amendment Dated September 9, 2003

Attorney Docket No. 81751.0017

holes 10 of Matsumoto are disposed in contact with silicon layer 3. Structures such as the insulating layer 9 are disposed between the silicon layer 3 and the eventual metal interconnections.

As shown in FIG. 2 of the Ko patent, the metal wire 142 is not disposed in contact with the surface silicon layer 100c. Structures such as the insulating layer 140 are disposed between the surface silicon layer 100c and the metal wire 142.

Applicant therefore respectfully submits that claim 1 is patentable over the cited references for at least the foregoing reasons. Applicant further submits that claims 2-6, 32, 33, and 38-40 are patentable at least by virtue of their dependency from claim 1.

Claims 7-13

To assist the Examiner in understanding how claim 7 reads on an embodiment of the invention shown, for example, in FIG. 8 Applicant has annotated claim 7 below. This embodiment is discussed, for example, at page 17, lines 17-20 of the specification. Applicant notes that the claims should not be construed as being limited to this embodiment, and that the annotation is provided only for the purpose of showing the Examiner how claim 7 reads on this embodiment. Amended claim 7 relates to a semiconductor device (FIG. 8), comprising:

a semiconductor substrate (320) having a contact region (322) provided therein;

an insulation layer (330) provided above the semiconductor substrate (320);

a semiconductor layer (340) provided above the insulation layer (330);
a conductive layer (362) disposed in contact with the semiconductor layer (360), wherein the conductive layer allows charge to flow into the semiconductor substrate (320), said contact region (322) being electrically connected to the conductive layer (362); and

a contact layer (360) provided in a first connection hole (350), the contact layer (360) electrically connecting the contact region (322) and the conductive layer (362). (Emphasis added.)

Application No. 09/943,094
Reply to Office Action of June 10, 2003
Amendment Dated September 9, 2003

Attorney Docket No. 81751.0017

Applicant submits that the cited references fail to teach or suggest, for example, "a conductive layer disposed in contact with the semiconductor layer, wherein the conductive layer allows charge to flow into the semiconductor substrate," as required by claim 7.

For example, as shown in FIG. 2 of the Wakahara reference, the silicon layer 1c is not in contact with the wiring 12d. Rather, structures such as the field insulating film 2 and the interlayer insulating film 10 are disposed between the silicon layer 1c and the wiring 12d.

There is nothing shown in FIGS. 4A and 4B of the Matsumoto reference that corresponds to the claimed "conductive layer." Moreover, neither the metal interconnections nor the conductive plugs that would eventually fill the contact holes 10 of Matsumoto are disposed in contact with silicon layer 3. Structures such as the insulating layer 9 are disposed between the silicon layer 3 and the eventual metal interconnections.

As shown in FIG. 2 of the Ko patent, the metal wire 142 is not disposed in contact with the surface silicon layer 100c. Structures such as the insulating layer 140 are disposed between the surface silicon layer 100c and the metal wire 142.

Applicant therefore respectfully submits that claim 7 is patentable over the cited references for at least the foregoing reasons. Applicant further submits that claims 8-11, 13, 34-35 and 41-43 are patentable at least by virtue of their dependency from claim 7.

Claims 14-19

To assist the Examiner in understanding how claim 14 reads on an embodiment of the invention shown, for example, in FIG. 5 Applicant has annotated claim 14 below. This embodiment is discussed, for example, at page 14, lines 10-16 of the specification. Applicant notes that the claims should not be construed as being limited to this embodiment, and that the annotation is provided only for the

Application No. 09/943,094
Reply to Office Action of June 10, 2003
Amendment Dated September 9, 2003

Attorney Docket No. 81751.0017

purpose of showing the Examiner how claim 14 reads on this embodiment. Amended claim 14 relates to a semiconductor device (FIG. 5), comprising:

a semiconductor substrate (220) having a first electrode (222) provided therein;

an insulation layer (230) provided above the semiconductor substrate(220);

a semiconductor layer (240) provided above the insulation layer (230), the semiconductor layer (240) a second electrode (244) provided therein, wherein the first electrode (222) is connected electrically to a conductive layer (262) disposed in contact with the semiconductor layer (240),

wherein the first electrode (222), the second electrode (244), and the insulation layer (230) are configured as a capacitive element.
(Emphasis added.)

Applicant submits that the cited references fail to teach or suggest, for example, that "the first electrode is connected electrically to a conductive layer disposed in contact with the semiconductor layer," as required by claim 14.

For example, as shown in FIG. 2 of the Wakahara reference, the silicon layer 1c is not in contact with the wiring 12d. Rather, structures such as the field insulating film 2 and the interlayer insulating film 10 are disposed between the silicon layer 1c and the wiring 12d. Moreover, the impurity semiconductor region 14, the wiring 12d, and the buried oxide layer 1b of Wakahara are not configured as a capacitive element.

Morihara also does not teach or suggest the limitations of claim 14.

Applicant therefore respectfully submits that claim 14 is patentable over the cited references for at least the foregoing reasons. Applicant further submits that claims 15-19, 36, 37 and 44 are patentable at least by virtue of their dependency from claim 14.

New dependent claims 32-44

New dependent claims 32-44 are added by this amendment. Applicant submits that these claims further define over the cited references since these claims

Application No. 09/943,094
Reply to Office Action of June 10, 2003
Amendment Dated September 9, 2003

Attorney Docket No. 81751.0017

recite additional features that are not taught or suggested by the cited references. Accordingly, Applicant submits that those claims are separately patentable over the cited references.

The art made of record but not relied upon by the Examiner has been considered. However, it is submitted that this art neither describes nor suggests the presently claimed invention.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6793 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: September 9, 2003

By: Erin P. Madill
Erin P. Madill
Registration No. 46,893
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701

RECEIVED
CENTRAL FAX CENTER

SEP 10 2003

OFFICIAL